1 Profile guided selection of ARM and thumb instructions
Arvind Krishnaswamy, Rajiv Gupta
July 2002 **LCTES/ SCOPES '02**: Proceedings of the joint conference on Languages, coi for embedded systems: software and compilers for embedded systems
Publisher: ACM
Full text available: Pdf (133.90 KB) Additional Information: full citation, abstract, references, citec

Bibliometrics: Downloads (6 Weeks): 8, Downloads (12 Months): 81, Citation Count: 21

The ARM processor core is a leading processor design for the embedded domain. In t domain, both memory and energy are important concerns. For this reason the 32 bit supports the 16 bit Thumb instruction set. For a given ...

Keywords: 16/32 bit instructions, code size and speed, low power

Also published in:
July 2002 **SIGPLAN Notices** Volume 37 Issue 7

2 Mixed-width instruction sets
Arvind Krishnaswamy, Rajiv Gupta
August 2003 **Communications of the ACM** , Volume 46 Issue 8
Publisher: ACM
Full text available: Html (28.62 KB), Pdf (110.18 KB) Additional Information: full citation, abstract, ref terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 57, Citation Count: 3

Encoding a program's computations to reduce memory and power consumption withc performance.

3 Enhancing the performance of 16-bit code using augmenting instructions
Arvind Krishnaswamy, Rajiv Gupta
July 2003 **LCTES '03**: Proceedings of the 2003 ACM SIGPLAN conference on Language for embedded systems
Publisher: ACM
Full text available: Pdf (276.13 KB) Additional Information: full citation, abstract, references, citec

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 25, Citation Count: 7

In the embedded domain, memory usage and energy consumption are critical constr instruction set embedded processors such as the ARM provide a 16-bit instruction set 32-bit instruction set to address these concerns. ...

Keywords: 16-bit thumb ISA, 32-bit ARM ISA, AX instructions, code size, embeddec instruction coalescing, performance

Also published in:
July 2003 **SIGPLAN Notices** Volume 38 Issue 7

4 Lessons learned in modeling schizophrenic and depressed responsive virtual hu
Robert C. Hubal, Geoffrey A. Frank, Curry I. Guinn
January 2003 **IUI '03: Proceedings of the 8th international conference on Intelligent use**
Publisher: ACM
Full text available: Pdf (355.06 KB) Additional Information: full citation, abstract, references, citec

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 53, Citation Count: 3

This paper describes lessons learned in developing the linguistic, cognitive, emotiona models underlying virtual human behavior in a training application designed to train officers how to recognize gestures and verbal cues ...

Keywords: agents, behavior modeling, interaction skills training, managing encount mentally ill, responsive virtual humans

5 Metrics for text entry research: an evaluation of MSD and KSPC, and a new unifi
R. William Soukoreff, I. Scott MacKenzie
April 2003 **CHI '03: Proceedings of the SIGCHI conference on Human factors in compu**
Publisher: ACM
Full text available: Pdf (549.73 KB) Additional Information: full citation, abstract, references, citec

Bibliometrics: Downloads (6 Weeks): 15, Downloads (12 Months): 102, Citation Count: 38

We describe and identify shortcomings in two statistics recently introduced to measu entry evaluations: the minimum string distance (MSD) error rate and keystrokes per To overcome the weaknesses, a new framework for ...

6 Lx: a technology platform for customizable VLIW embedded processing
Paolo Faraboschi, Geoffrey Brown, Joseph A. Fisher, Giuseppe Desoli, Fred Homewood
June 2000 **ISCA '00: Proceedings of the 27th annual international symposium on Comp**
Publisher: ACM
Full text available: Pdf (344.41 KB) Additional Information: full citation, abstract, references, citec

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 63, Citation Count: 81

Lx is a scalable and customizable VLIW processor technology platform designed by H STMicroelectronics that allows variations in instruction issue width, the number and c structures and the processor instruction set. For ...

Also published in:
May 2000 **SIGARCH Computer Architecture News** Volume 28 Issue 2

7 A New Algorithm for Energy-Driven Data Compression in VLIW Embedded Proce
Alberto Macii, Enrico Macii, Fabrizio Crudo, Roberto Zafalon
March 2003 **DATE '03: Proceedings of the conference on Design, Automation and Volume 1** , Volume 1
Publisher: IEEE Computer Society
Full text available: Publisher Site , Pdf (113.19 KB) Additional Information: full citation, abstract, refe terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 12, Citation Count: 2

This paper presents a new algorithm for on-the-fly data compression in high perform processors. The algorithm aggressively targets energy minimization of some of the d the SoC energy budget (i.e., main memory access and high ...

Keywords: Data compression algorithms, system-level energy optimization, VLIW e processors

8 Control Flow Driven Splitting of Loop Nests at the Source Code Level
Heiko Falk, Peter Marwedel
March 2003 **DATE '03: Proceedings of the conference on Design, Automation and Volume 1** , Volume 1
Publisher: IEEE Computer Society
Full text available: Publisher Site , Pdf (215.57 KB) Additional Information: full citation, abstract, refe terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 14, Citation Count: 6

This paper presents a novel source code transformation for control flow optimization splitting which minimizes the number of executed if-statements in loop nests of emb applications. The goal of the optimization is to ...

9 System-level power optimization: techniques and tools
Luca Benini, Giovanni De Micheli
August 1999 **ISLPED '99: Proceedings of the 1999 international symposium on Low pow design**
Publisher: ACM
Full text available: Pdf (663.71 KB) Additional Information: full citation, references, cited by, inde

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 32, Citation Count: 13

10 A case for fractured mirrors
Ravishankar Ramamurthy, David J. DeWitt, Qi Su
August 2003 **The VLDB Journal — The International Journal on Very Large Data B** 2
Publisher: Springer-Verlag New York, Inc.
Full text available: Pdf (200.49 KB) Additional Information: full citation, abstract, references, citec

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 24, Citation Count: 3

Abstract.The decomposition storage model (DSM) vertically partitions all attributes o excellent I/O behavior when the number of attributes accessed by a query is small. I cache footprint than the standard storage model ...

Keywords: Data placement, Disk mirroring, Vertical partitioning

11 An efficient technique for exploring register file size in ASIP synthesis
Manoj Kumar Jain, M. Balakrishnan, Anshul Kumar
October 2002 **CASES '02: Proceedings of the 2002 international conference on Compiler synthesis for embedded systems**
Publisher: ACM
Full text available: Pdf (244.65 KB) Additional Information: full citation, abstract, references, citec

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 23, Citation Count: 2

Performance estimation is a crucial operation which drives the design space explorati Specific Instruction Set Processors (ASIP) synthesis. The usual approach to estimate do simulation. With increasing dimensions of ...

Keywords: ASIP Synthesis, design space exploration, global analysis, instruction sc analysis, register file, register spill, retargetable estimation, storage exploration

12

Survey of code-size reduction methods
Árpád Beszédes, Rudolf Ferenc, Tibor Gyimóthy, André Dolenc, Konsta Karsisto
September 2003 **Computing Surveys (CSUR)** , Volume 35 Issue 3
Publisher: ACM
Full text available: Pdf (443.89 KB) Additional Information: full citation, abstract, references, citec

Bibliometrics: Downloads (6 Weeks): 29, Downloads (12 Months): 266, Citation Count: 14

Program code compression is an emerging research activity that is having an impact production areas such as networking and embedded systems. This is because the rec can have a positive impact on network traffic and embedded ...

Keywords: code compaction, code compression, method assessment, method evalu

13 A practical dynamics system
Zoran Kačić-Alesić, Marcus Nordenstam, David Bullock
July 2003 **SCA '03:** Proceedings of the 2003 ACM SIGGRAPH/Eurographics symposium animation
Publisher: Eurographics Association
Full text available: Pdf (3.22 MB) Additional Information: full citation, abstract, references, citec

Bibliometrics: Downloads (6 Weeks): 23, Downloads (12 Months): 118, Citation Count: 6

We present an effective production-proven dynamics system. It uses an explicit time method that is efficient, reasonably accurate, conditionally stable, and above all simp We describe issues related to integration of physically ...

14 Patchable instruction ROM architecture
Timothy Sherwood, Brad Calder
November 2001 **CASES '01:** Proceedings of the 2001 international conference on Compil and synthesis for embedded systems
Publisher: ACM
Full text available: Pdf (299.03 KB) Additional Information: full citation, abstract, references, inde

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 33, Citation Count: 0

Increased systems level integration has meant the movement of many traditionally o onto a single chip including a processor, instruction storage, data path, and local mer these systems is driven by two conflicting ...

15 CMIFed: a presentation environment for portable hypermedia documents
Guido van Rossum, Jack Jansen, K. Sjoerd Mullender, Dick C. A. Bulterman
September 1993 **MULTIMEDIA '93:** Proceedings of the first ACM international conferenc
Publisher: ACM
Full text available: Pdf (175.93 KB), Ps (867.94 KB) Additional Information: full citation, references, c

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 30, Citation Count: 29

Keywords: CMIF, editing environment, heterogeneity, hypermedia, multimedia, port synchronization

16 A DISE implementation of dynamic code decompression
Marc L. Corliss, E. Christopher Lewis, Amir Roth
July 2003 **LCTES '03:** Proceedings of the 2003 ACM SIGPLAN conference on Language for embedded systems
Publisher: ACM
Full text available: Pdf (291.52 KB) Additional Information: full citation, abstract, references, citec

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 14, Citation Count: 11

Code compression coupled with dynamic decompression is an important technique fo and general-purpose microprocessors. *Post-fetch decompression*, in which decompre after the compressed instructions have been fetched, ...

Keywords: DISE, code compression, code decompression

Also published in:
July 2003 **SIGPLAN Notices** Volume 38 Issue 7

17 A design space exploration framework for reduced bit-width instruction set archit design
Ashok Halambi, Aviral Shrivastava, Partha Biswas, Nikil Dutt, Alex Nicolau
October 2002 **ISSS '02**: Proceedings of the 15th international symposium on System Sy
Publisher: ACM
Full text available: Pdf (137.08 KB) Additional Information: full citation, abstract, references, citec

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 19, Citation Count: 1

Code size is a critical concern in many embedded system applications, especially thos One promising approach for reducing code size is to employ a "dual instruction set", architectures support a normal (usually 32 bit) ...

Keywords: compressed instruction set, design space exploration, dual Instruction se bit-width instruction set, register pressure, thumb

18 System architecture directions for networked sensors
Jason Hill, Robert Szewczyk, Alec Woo, Seth Hollar, David Culler, Kristofer Pister
November 2000 **SIGPLAN Notices**, Volume 35 Issue 11
Publisher: ACM
Full text available: Pdf (1.32 MB) Additional Information: full citation, abstract, references, citec

Bibliometrics: Downloads (6 Weeks): 38, Downloads (12 Months): 381, Citation Count: 23

Technological progress in integrated, low-power, CMOS communication devices and s rich design space of networked sensors viable. They can be deeply embedded in the spread throughout our environment like smart dust. The ...

19 A codesigned on-chip logic minimizer
Roman Lysecky, Frank Vahid
October 2003 **CODES+ISSS '03**: Proceedings of the 1st IEEE/ACM/IFIP international cor Hardware/software codesign and system synthesis
Publisher: ACM
Full text available: Pdf (225.60 KB) Additional Information: full citation, abstract, references, citec

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 23, Citation Count: 6

Boolean logic minimization is traditionally used in logic synthesis tools running on po computers. However, logic minimization has recently been proposed for dynamic use systems, including network route table reduction, network ...

Keywords: dynamic optimization, embedded CAD, embedded systems, hardware/so logic minimization, on-chip logic minimization, on-chip synthesis, system-on-a-chip

20 Peephole displays: pen interaction on spatially aware handheld computers
Ka-Ping Yee
April 2003 **CHI '03**: Proceedings of the SIGCHI conference on Human factors in compu

Publisher: ACM
Full text available: Pdf (6.59 MB) Additional Information: full citation, abstract, references, citec

Bibliometrics: Downloads (6 Weeks): 16, Downloads (12 Months): 126, Citation Count: 43

The small size of handheld computers provides theconvenience of mobility at the exp screen space for display and interaction. Prior research has identified the value of spa displays, in which a position-tracked display provides ...

Keywords: 3-D drag-and-drop, mobile computing, personal information spaces, spa displays, two-handed interaction

Result page: 1